IN THE CLAIMS

Please cancel claims 41 and 60, amend claims 39, 42, and 59, 61 and 62, and add new claims 63-65, as indicated below.

1-38. (Cancelled)

39. (Currently Amended) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including at least first and second inputs each coupled to sample a signal, wherein at least the first input is coupled to the signal path at an interior node of the amplifier that is disposed between, but is exclusive of, the input and the output of the amplifier, and the power detector circuit is operable to output a first signal reflective of the signal sampled at the at least first and second inputs,

wherein the second input of the power detector circuit is coupled to sample at a second interior node of the amplifier, the second interior node also being disposed between, but exclusive of, the input and the output of the amplifier.

40. (Previously Added) The amplifier circuit of claim 39 further comprising at least one intermediate said amplifier stage in the signal path between the first and second amplifiers,

wherein the first input is coupled for sampling between either the first amplifier stage and the at least one intermediate amplifier stage or between the at least one intermediate amplifier stage and the final amplifier stage.

41. (Cancelled)

42. (Currently Amended) The amplifier circuit of claim ~~41~~ 40, wherein the amplifier comprises a final said amplifier stage having an output, and an output matching network having an input coupled to the output of the final amplifier stage and an output that forms the output of the amplifier.

43. (Previously Added) The amplifier circuit of claim 39, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the interior node is within the matching network.

44. (Previously Added) The amplifier circuit of claim 39, further comprising a bias circuit, wherein the bias circuit provides a DC bias signal to at least one of the first and second amplifier stages, the bias signal depending, at least in part, on the first signal.

45. (Previously Added) The amplifier circuit of claim 44, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the interior node is within the matching network.

46. (Previously Added) The amplifier circuit of claim 39, further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the first stage, the bias signal depending, at least in part, on the first signal.

47. (Previously Added) The amplifier circuit of claim 39, wherein the first signal reflects a summing of signals derived from the sampling at the at least first and second inputs.

48. (Previously Added) The amplifier circuit of claim 39, wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

49. (Previously Added) The amplifier circuit of claim 39, wherein the first signal reflects a greater weight given to a signal derived from the sampling at one of the first and second inputs than to a signal derived from the sampling at other of the first and second inputs.

50. (Previously Added) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including at least first and second inputs each coupled to sample a signal, wherein the first and second inputs are each coupled to the signal path at first and second interior nodes, respectively, of the amplifier, the first and second interior nodes being disposed between, but exclusive of, the input and the output of the amplifier, and the power detector circuit is operable to output a first signal reflective of the signal sampled at the at least first and second inputs.

51. (Previously Added) The amplifier circuit of claim 50, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node comprises is within the matching network.

52. (Previously Added) The amplifier circuit of claim 50, further comprising a bias circuit, wherein the bias circuit provides a DC bias signal to at least one of the first and second amplifier stages, the bias signal depending, at least in part, on the first signal.

53. (Previously Added) The amplifier circuit of claim 52, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node is within the matching network.

54. (Previously Added) The amplifier circuit of claim 50, further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the first amplifier stage, the bias signal depending, at least in part, on the first signal.

55. (Previously Added) The amplifier circuit of claim 50, further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the second amplifier stage, the bias signal depending, at least in part, on the first signal.

56. (Previously Added) The amplifier circuit of claim 50, wherein the first signal reflects a summing of signals derived from the sampling at the at least first and second inputs.

57. (Previously Added) The amplifier circuit of claim 50, wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

58. (Previously Added) The amplifier circuit of claim 50, wherein the first signal reflects a greater weight given to a signal derived from the sampling at one of the first and second inputs than to a signal derived from the sampling at the other of the first and second inputs.

59. (Currently Amended) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior said node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior said node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the sampling includes sampling at a second interior said node on the signal path, the second interior said node being between, but exclusive of, the input and output of the amplifier.

60. (Cancelled)

61. (Currently Amended) The method of claim ~~60~~ 59, wherein the first signal is formed by summing signals derived from the sampling.

62. (Currently Amended) The method of claim ~~60~~ 59, wherein the first signal is formed based on a difference between signals derived from the sampling.

63. (Re-presented - Formerly claim 48) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including at least first and second inputs each coupled to sample a signal, wherein at least the first input is coupled to the signal path at an interior node of the amplifier that is disposed between, but is exclusive of, the input and the output of the amplifier, and the power detector circuit is operable to output a first signal reflective of the signal sampled at the at least first and second inputs,

wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

64. (Re-presented - Formerly claim 61) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the

input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior said node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior said node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the first signal is formed by summing signals derived from the sampling.

65. (Re-presented - Formerly claim 62) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior said node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior said node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the first signal is formed based on a difference between signals derived from the sampling.